FIG.1 PRIOR ART

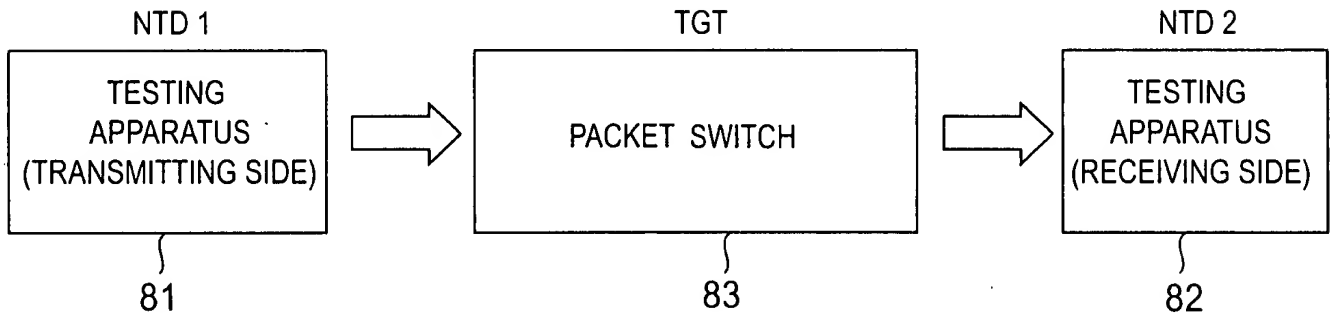


FIG.2 PRIOR ART

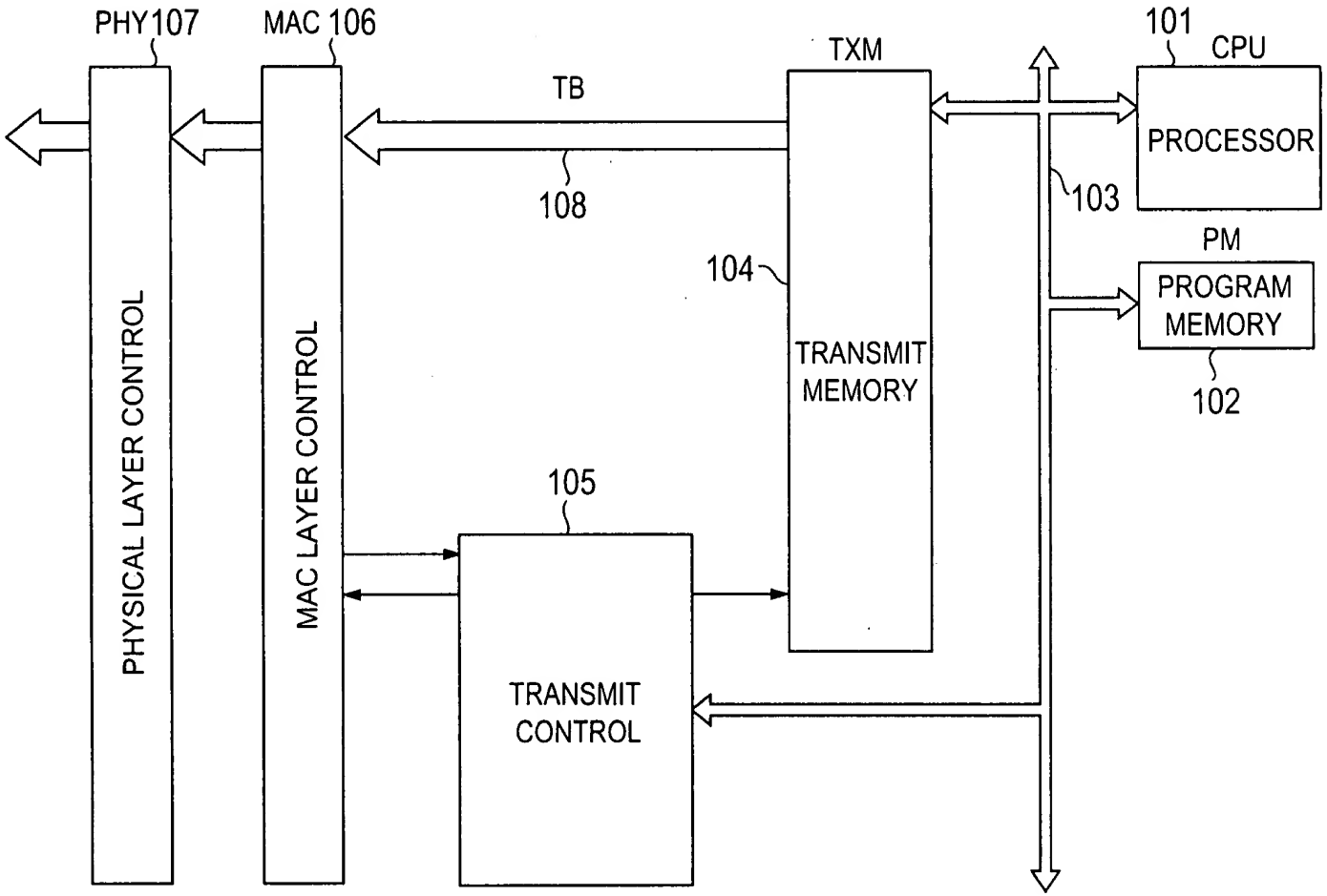


FIG.3 PRIOR ART

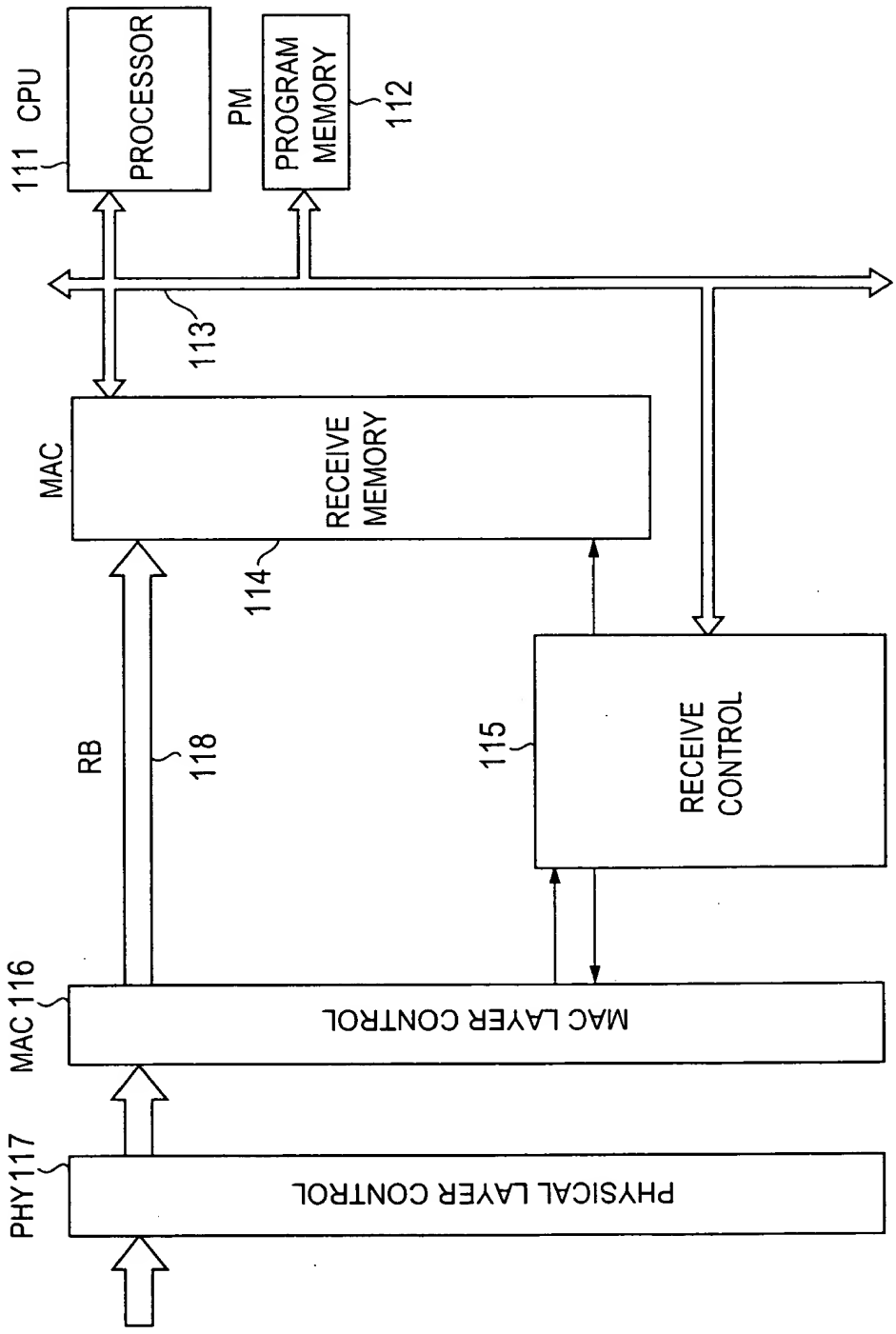


FIG.4

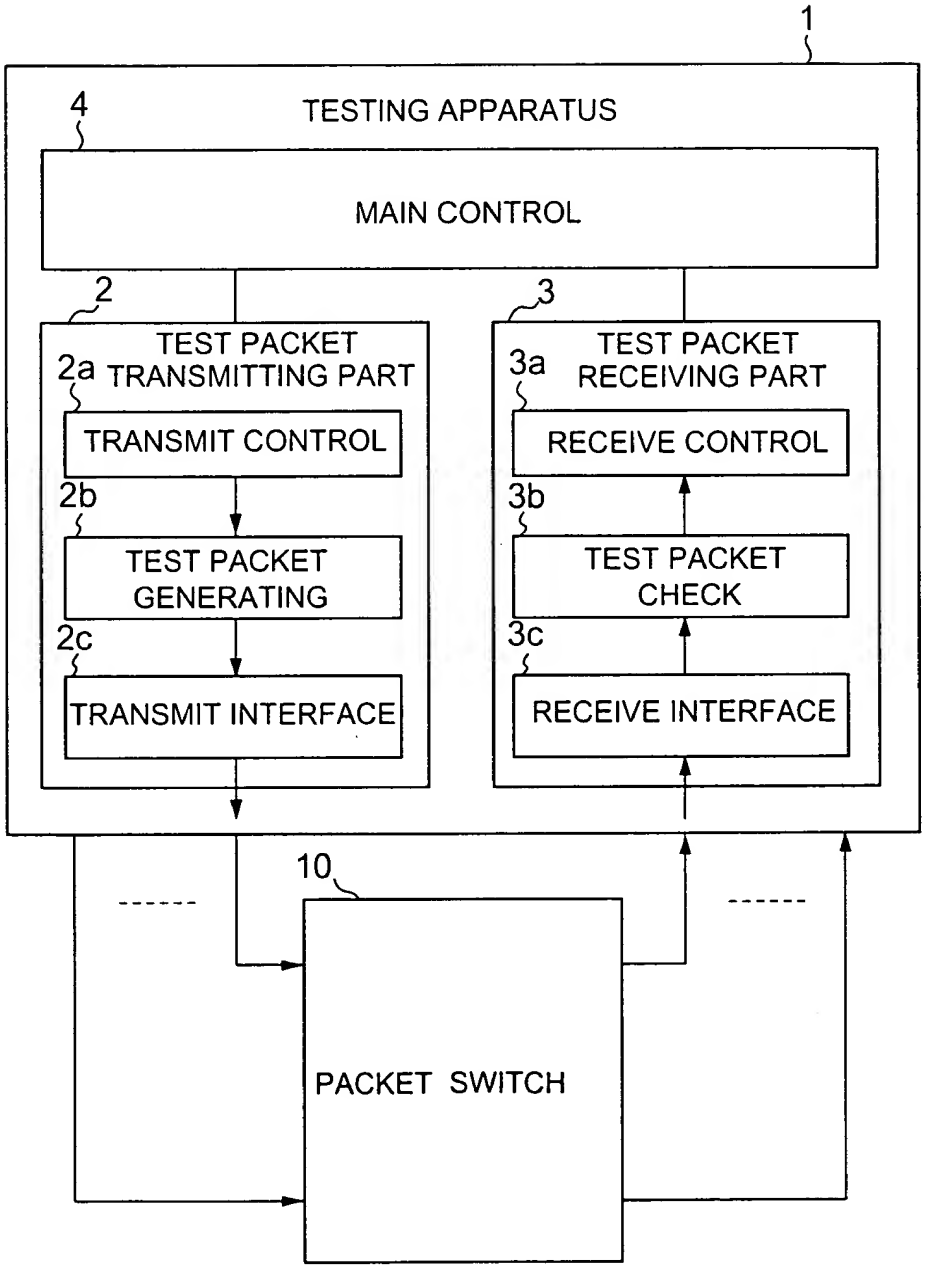

1
4
TESTING APPARATUS
MAIN CONTROL
2
TEST PACKET TRANSMITTING PART
2a
TRANSMIT CONTROL
2b
TEST PACKET GENERATING
2c
TRANSMIT INTERFACE
3
TEST PACKET RECEIVING PART
3a
RECEIVE CONTROL
3b
TEST PACKET CHECK
3c
RECEIVE INTERFACE
10
PACKET SWITCH

FIG.5

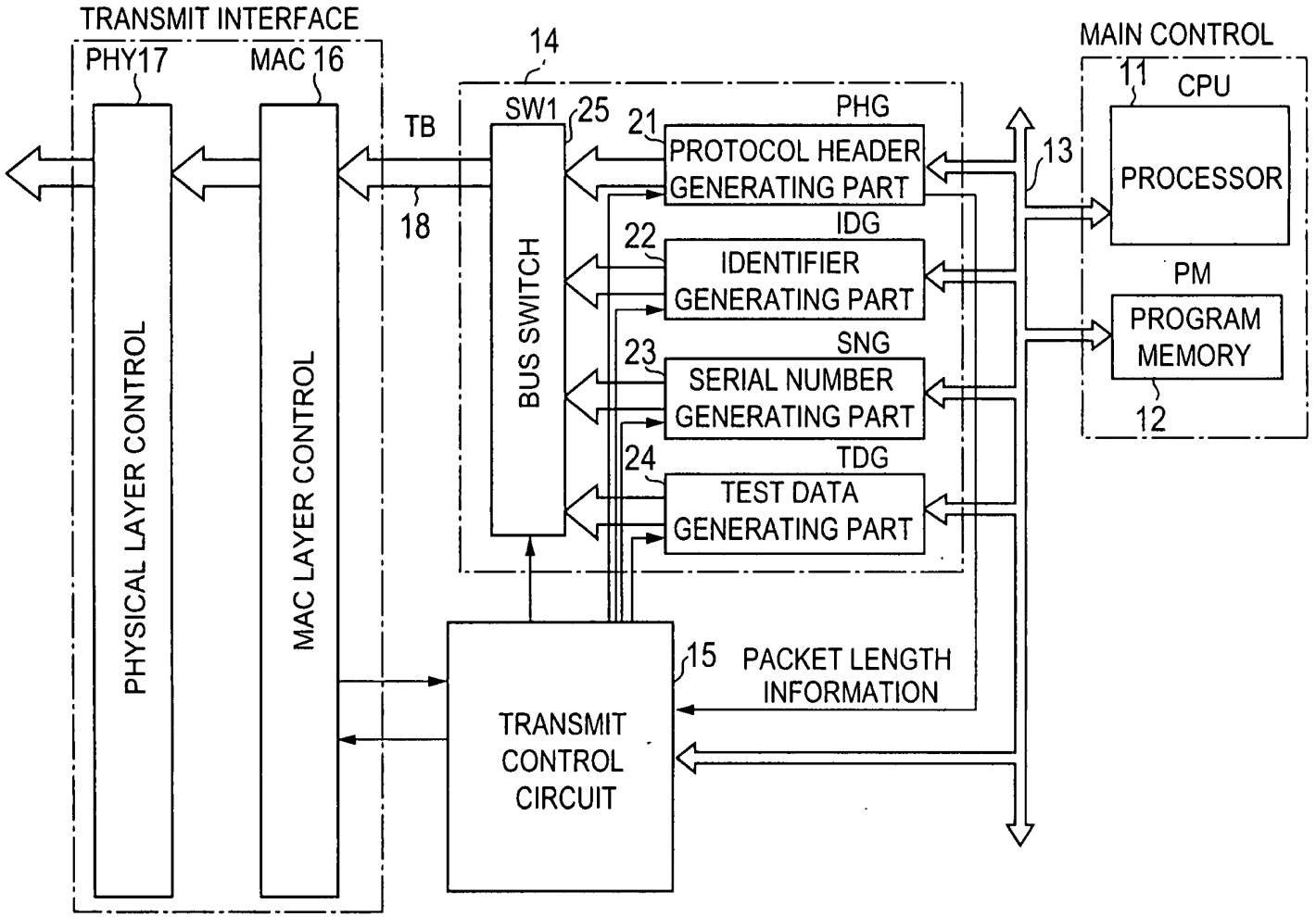


FIG.6A

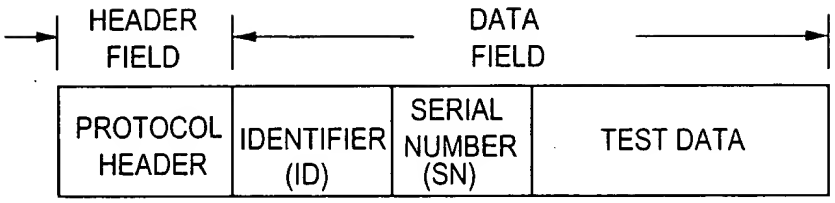

HEADER FIELD
DATA FIELD
PROTOCOL HEADER
IDENTIFIER (ID)
SERIAL NUMBER (SN)
TEST DATA

FIG.6B

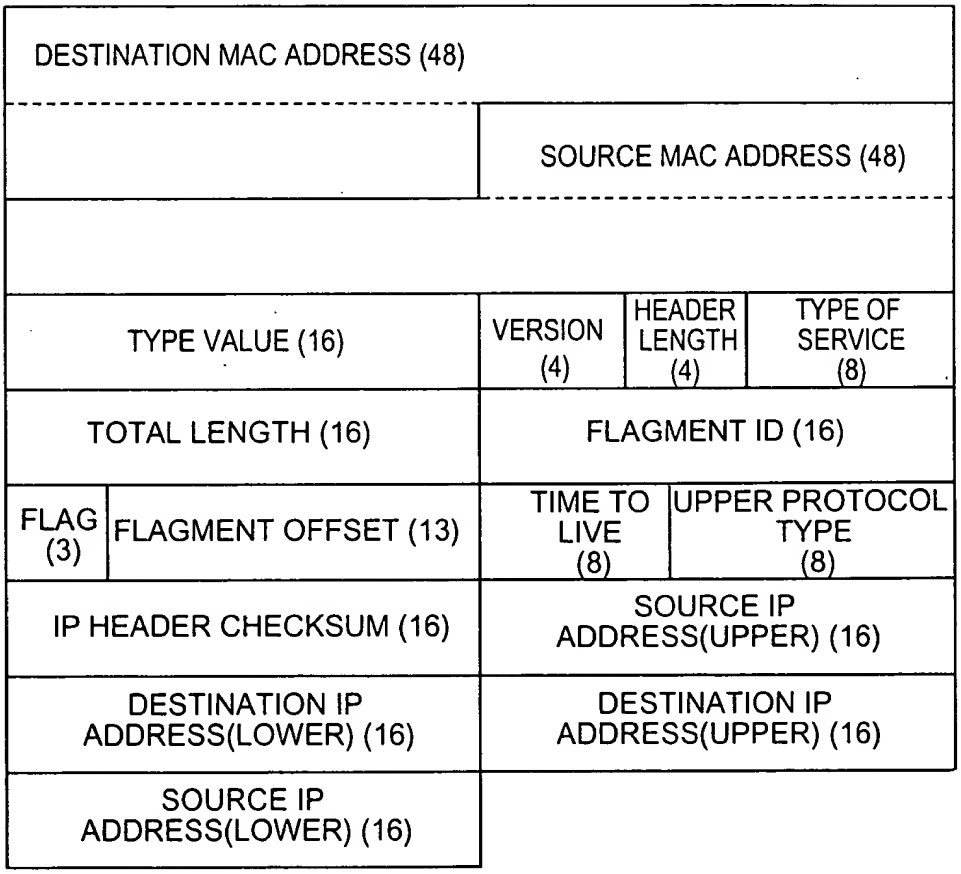

DESTINATION MAC ADDRESS (48)
SOURCE MAC ADDRESS (48)
TYPE VALUE (16)
VERSION (4)
HEADER LENGTH (4)
TYPE OF SERVICE (8)
TOTAL LENGTH (16)
FLAGMENT ID (16)
FLAG (3)
FLAGMENT OFFSET (13)
TIME TO LIVE (8)
UPPER PROTOCOL TYPE (8)
IP HEADER CHECKSUM (16)
SOURCE IP ADDRESS(UPPER) (16)
DESTINATION IP ADDRESS(LOWER) (16)
DESTINATION IP ADDRESS(UPPER) (16)
SOURCE IP ADDRESS(LOWER) (16)

FIG.7

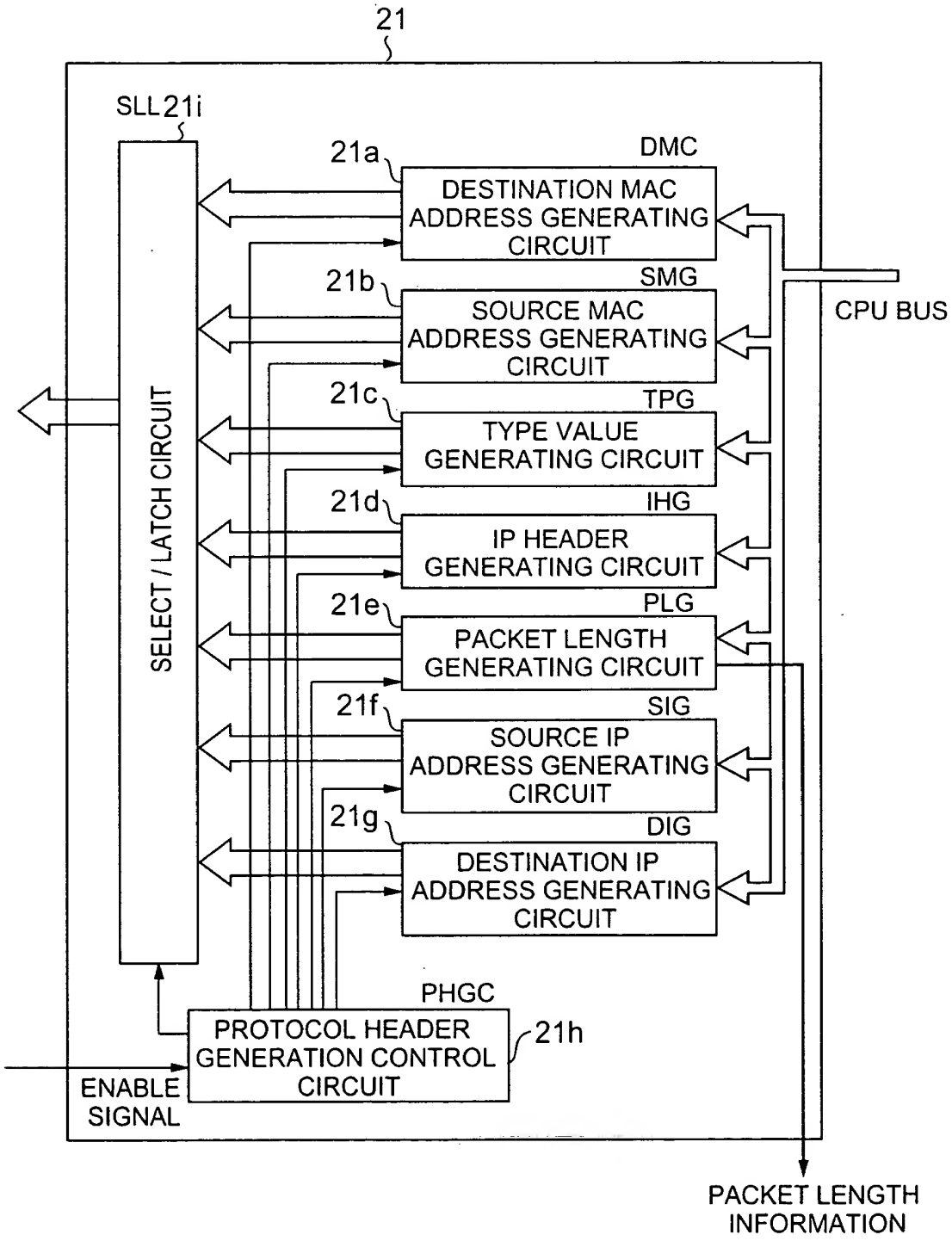

21
SLL 21i
SELECT / LATCH CIRCUIT
21a
DMC
DESTINATION MAC ADDRESS GENERATING CIRCUIT
21b
SMG
SOURCE MAC ADDRESS GENERATING CIRCUIT
21c
TPG
TYPE VALUE GENERATING CIRCUIT
21d
IHG
IP HEADER GENERATING CIRCUIT
21e
PLG
PACKET LENGTH GENERATING CIRCUIT
21f
SIG
SOURCE IP ADDRESS GENERATING CIRCUIT
21g
DIG
DESTINATION IP ADDRESS GENERATING CIRCUIT
PHGC
PROTOCOL HEADER GENERATION CONTROL CIRCUIT
21h
ENABLE SIGNAL
CPU BUS
PACKET LENGTH INFORMATION

FIG.8

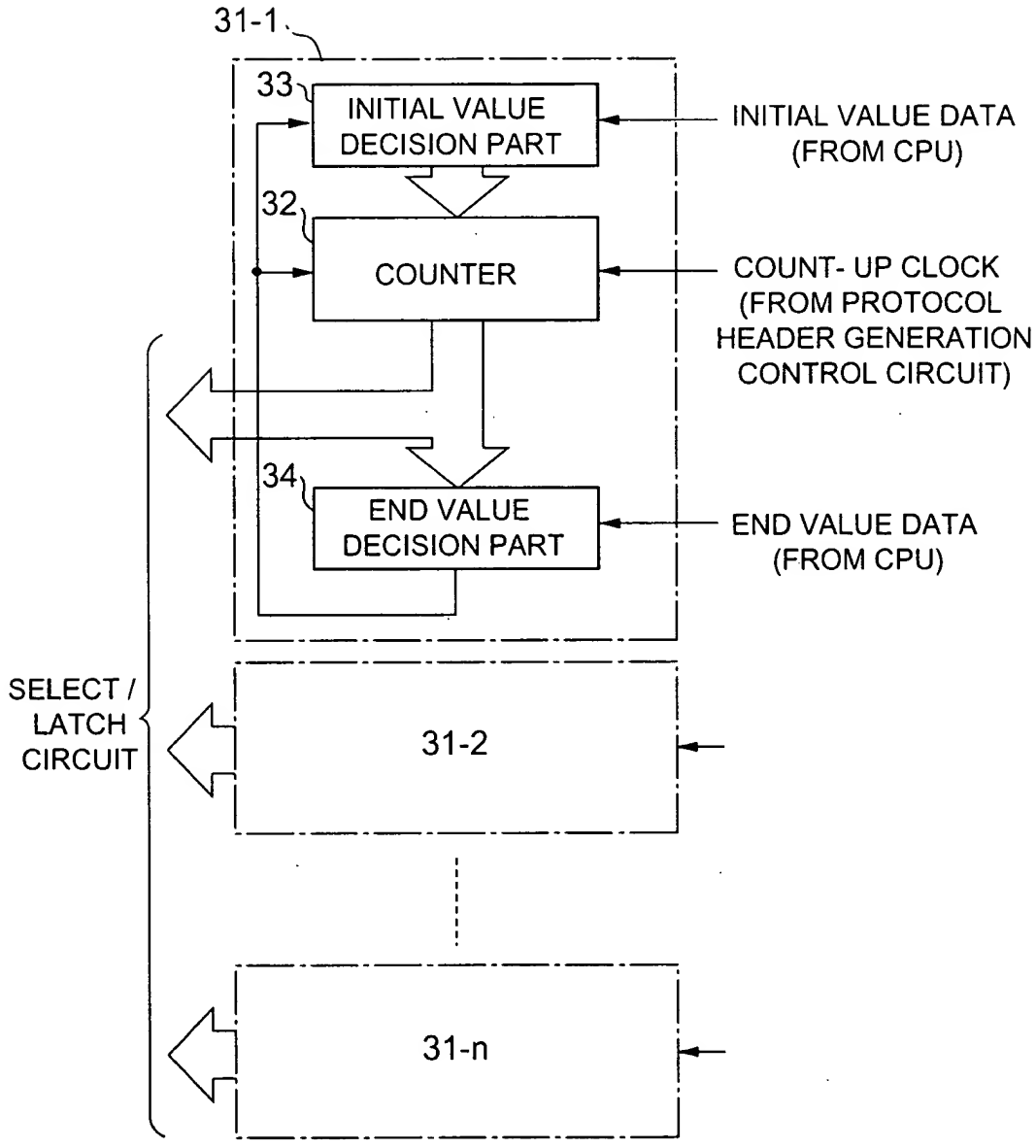

31-1
33
INITIAL VALUE DECISION PART
INITIAL VALUE DATA (FROM CPU)
32
COUNTER
COUNT- UP CLOCK (FROM PROTOCOL HEADER GENERATION CONTROL CIRCUIT)
34
END VALUE DECISION PART
END VALUE DATA (FROM CPU)
SELECT / LATCH CIRCUIT
31-2
31-n

FIG.9

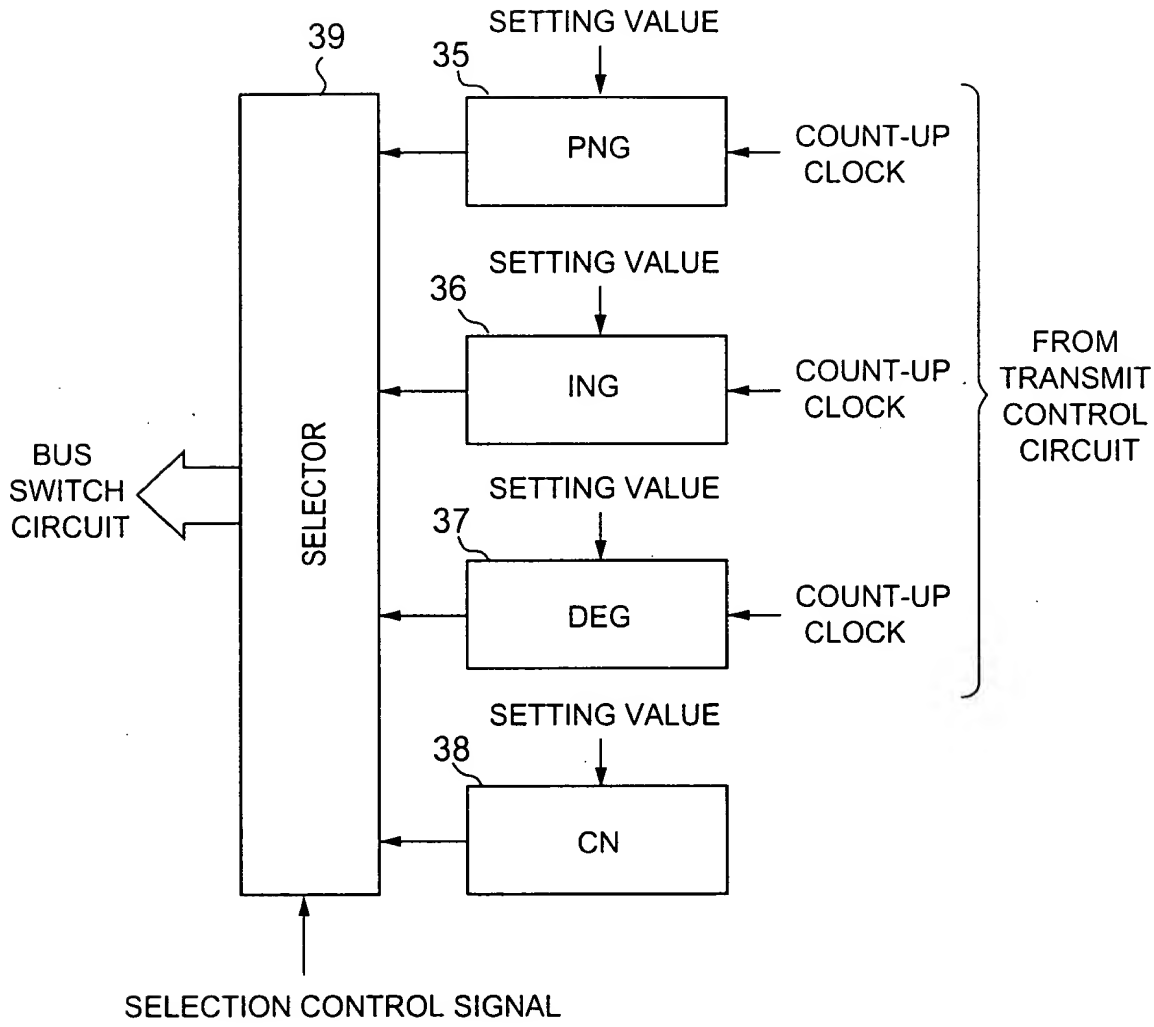

39
SETTING VALUE
35
PNG
COUNT-UP CLOCK
SETTING VALUE
36
ING
COUNT-UP CLOCK
FROM TRANSMIT CONTROL CIRCUIT
BUS SWITCH CIRCUIT
SELECTOR
SETTING VALUE
37
DEG
COUNT-UP CLOCK
SETTING VALUE
38
CN
SELECTION CONTROL SIGNAL

FIG.10

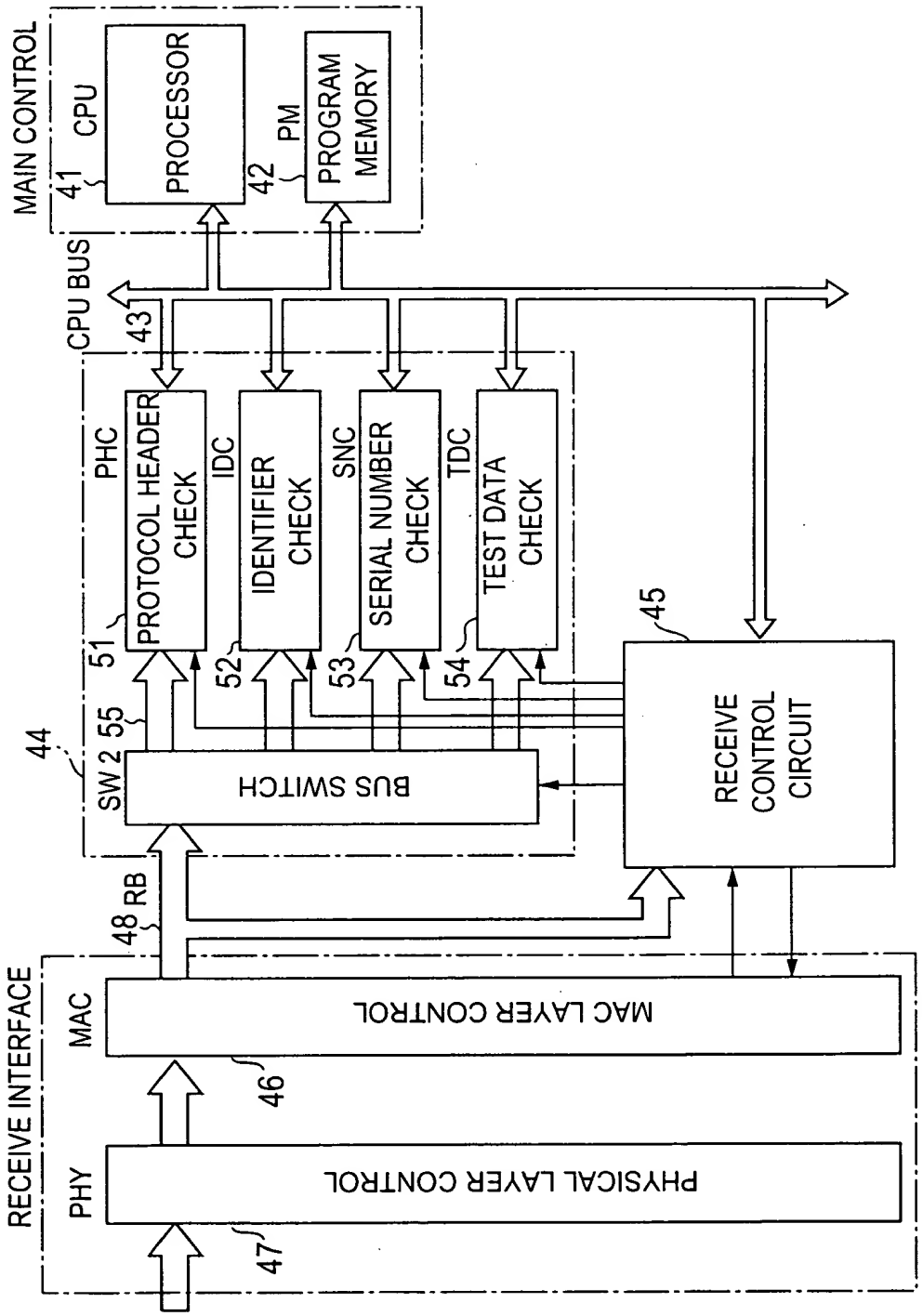
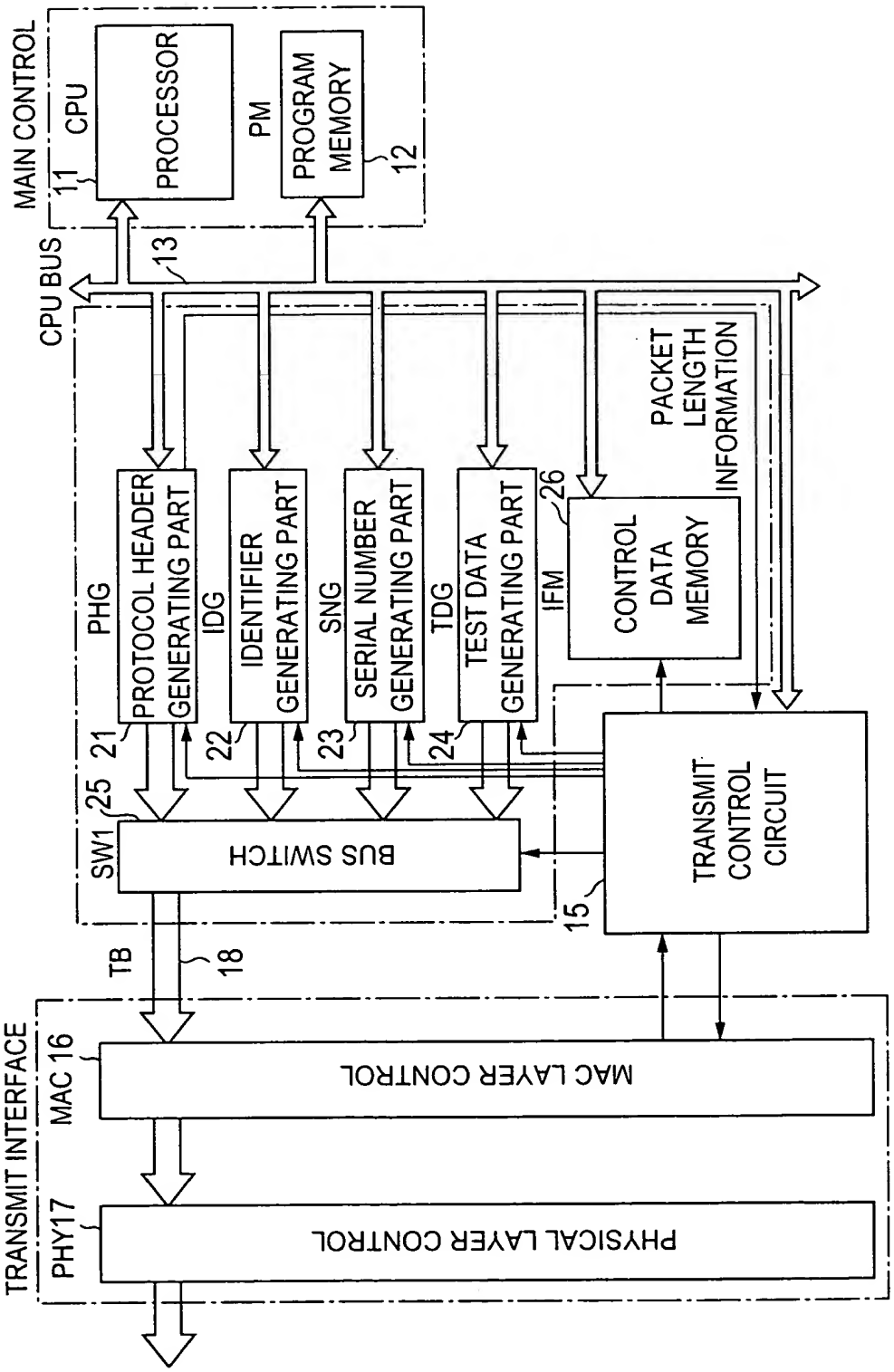

MAIN CONTROL
CPU
41
PROCESSOR
PM
42
PROGRAM MEMORY
CPU BUS
43
PHC
PROTOCOL HEADER CHECK
51
IDC
IDENTIFIER CHECK
52
SNC
SERIAL NUMBER CHECK
53
TDC
TEST DATA CHECK
54
45
RECEIVE CONTROL CIRCUIT
44
SW 2
55
BUS SWITCH
48
RB
RECEIVE INTERFACE
MAC
MAC LAYER CONTROL
46
PHY
PHYSICAL LAYER CONTROL
47

FIG.11


MAIN CONTROL
CPU
11
PROCESSOR
PM
PROGRAM MEMORY
12
CPU BUS
13
PACKET LENGTH INFORMATION
PHG
PROTOCOL HEADER GENERATING PART
21
IDG
IDENTIFIER GENERATING PART
22
SNG
SERIAL NUMBER GENERATING PART
23
TDG
TEST DATA GENERATING PART
24
IFM
26
CONTROL DATA MEMORY
SW1
25
BUS SWITCH
TRANSMIT CONTROL CIRCUIT
15
TB
18
TRANSMIT INTERFACE
MAC 16
MAC LAYER CONTROL
PHY17
PHYSICAL LAYER CONTROL